CLAIMS

1. An integrated circuit comprising a processor, a memory that the processor can access, a memory access unit for controlling accesses to the memory, an input for receiving power for the integrated circuit from an external power source, and a power detection unit, the power detection unit being configured to:

monitor a quality of power supplied to the input;

in the event the quality of the power drops below a predetermined threshold, disabling a power supply to circuitry for use in writing to the memory, such that the memory access unit's ability to alter data in the memory is disabled prior to address or data values to be written to the memory becoming unreliable due to failing power.

2. An integrated circuit according to claim 1, wherein the memory is flash memory and the power supply is one or more charge pump circuits.

3. An integrated circuit according to claim 2, wherein a voltage output by the power supply falls fast enough that the voltage supplied to the flash memory becomes too low to enable a change in contents of the flash memory before the voltage levels of the address or data values become invalid.

4. An integrated circuit according to claim 1, configured to cause a reset of at least some of the circuitry on the integrated circuit following disabling of the power supply.

5. An integrated circuit according to claim 4, programmed or designed to have a variable delay between disabling of the power supply and causing the reset.